Heterogeneous Multi-Die Stitching: Technology Demonstration and Design Considerations

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***Abstract*— In this paper, a Heterogeneous Interconnect Stitching Technology (HIST) is reported. In the proposed approach, stitch-chips, which may be active or passive chips, are placed between the package substrate and concatenated 'anchor chips'. Fine-pitch Compressible MicroInterconnects (CMIs) are used to provide low-loss and robust interconnection between the anchor chips and the stitch-chips. The CMIs are also used to compensate for any package non-planarity and stitch-chip thickness variations, as one anchor chip may interface to multiple different stitch-chips at each of its edges. Electrical measurements of the assembled chips are reported and demonstrate robust interconnection. Integrated circuits in the HIST platform are thermally evaluated to investigate thermal challenges and opportunities for such multi-die packages. Impact of different parameters, including die-spacing, stitch-chip splitting, and die-thickness mismatch, for example, on the thermal profile are evaluated. Moreover, power delivery network analysis is performed for the HIST platform with focus primarily on the IR-drop as a function of the overlap area between the anchor dice and the stitch-chips.**

Keywords-System-in-Package, compliant interconnects, 2.5D/3D package assembly, heterogeneous integration

I. INTRODUCTION

The explosive growths in the mobile and telecommunication markets have pushed the semiconductor industry towards ever more complex and sophisticated monolithic system-on-chip (SoC) solutions [1], [2]. Ever more advanced CMOS technology has enabled this integration, but has also led to a rise in design complexity, time, and costs [3], [4]. To enhance overall system flexibility and reduce design time and cost, heterogeneous integration of multi-dice manufactured using preferred processes from different foundries may provide benefits so long as one can provide high-density and low-loss interconnections [5]. As candidate solutions, both 2.5D integration and 3D integration design and manufacturing flows currently exist (for example, 3D stacked high-bandwidth memory and 2.5D silicon interposer technology) [6]-[13], but these technologies have limitations. There remains a need for low-loss and high-density integration solutions using low-cost off-chip interconnects to enable seamless integration of building blocks (i.e., IP blocks) at the 'off-chip-level.'

In this paper, we explore a heterogeneous multi-die stitching technology to enable concatenation of ICs using heterogeneous dice. Fig. 1 illustrates a schematic of the proposed technology, which we call Heterogeneous Interconnect Stitching Technology (HIST): specially, this is a second generation of a previously reported approach [14]. Stitch-chips with high-density interconnects are placed between the package substrate and the concatenated 'anchor chips'. The anchor chips can be logic, FPGA, memory, MMIC, photonic, or sensor dice, for example. Fine-pitch Compressible MicroInterconnects (CMIs) are used to provide high-density interfaces between the anchor chips and the stitch-chips. Solder bumps, with larger pitch and height, are used for power delivery, signal routing, and mechanical interconnection between the anchor chips and the package. The benefits of HIST are the following: First, HIST provides low-loss interconnects and improved thermal handling (due to access to air-cooled or microfluidic cooled heat sinks), which directly benefit high-power modules, such as power amplifier (PA), by improving their power efficiency, output power, thermal reliability, and device aging issues. Second, HIST allows the interconnection of multiple active chips with stitch-chips at tight signal pitches. Third, the fine-pitch CMIs can mechanically compensate for any substrate non-planarity and stitch-chip thickness variations, which could be challenging using conventional bump solutions as one anchor chip could be interfaced to multiple different stitch-

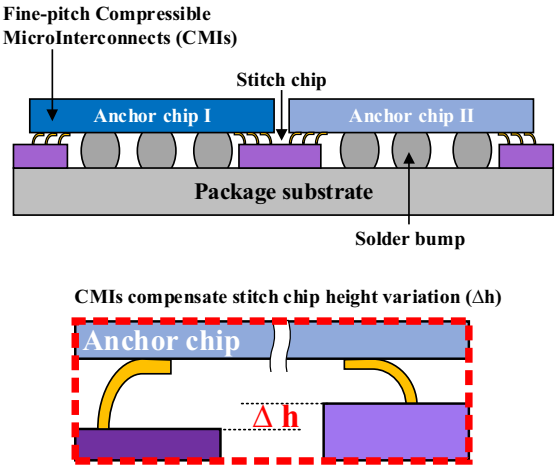

Fig. 1. HIST platform schematic

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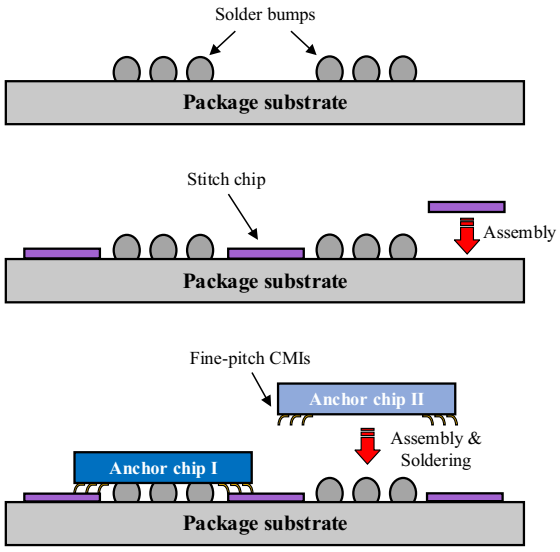


Fig. 2. The integration process flow

chips at each of its edges (especially for fine-pitch interconnects). Furthermore, the stitch-chip can be silicon, glass, or any other material based on need, and the stitch-chip may be an active IC and/or contain passive devices.

This paper is organized as follows: Section II describes the fabrication and assembly process of HIST and reports the DC resistance of the solder bumps and the CMIs. In Section III, a stitch-chip based 2.5D configuration is thermally evaluated. Section IV presents a power delivery analysis of multi-die packages using HIST. Finally, in Section V, concluding remarks are stated.

II. Fabrication, Assembly Process and Electrical Characterization

Fig. 2 shows the overall integration process flow of HIST. Firstly, solder bumps are batch fabricated on the package substrate (though, they can be formed on the dice). Next, the singulated stitch-chips with fine-pitch interconnects are assembled onto the package substrate. Lastly, the anchor chips with fine-pitch CMIs are flip-chip bonded onto the package substrate by reflowing the solder bumps. During the fabrication of the CMIs, NiW is used since it has high yield strength of 1.93 GPa; for reference, electroplated Cu has a reported yield strength of 136 MPa [15]. This high yield strength enables the CMI to tolerate more stress before experiencing plastic deformation during compression. The NiW CMIs are electroless gold plated at the end of the fabrication process to prevent oxidation. The fabrication process of the CMIs is described in [15]. In this paper, a testbed is fabricated and assembled in order to demonstrate the key features of the proposed HIST platform: assembly of anchor chips with fine-pitch CMIs onto a substrate with stitch-chips and solder bumps.

In the testbed, a stitch-chip on the package substrate is emulated by making a 20 µm tall step (though a larger step is

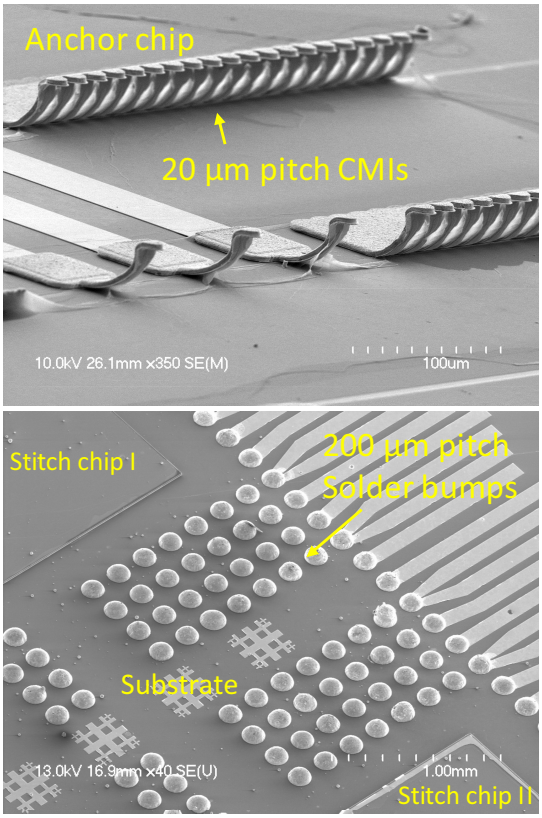


Fig. 3. SEM images of the solder bumps and fine-pitch CMIs on the substrate and anchor chip, respectively

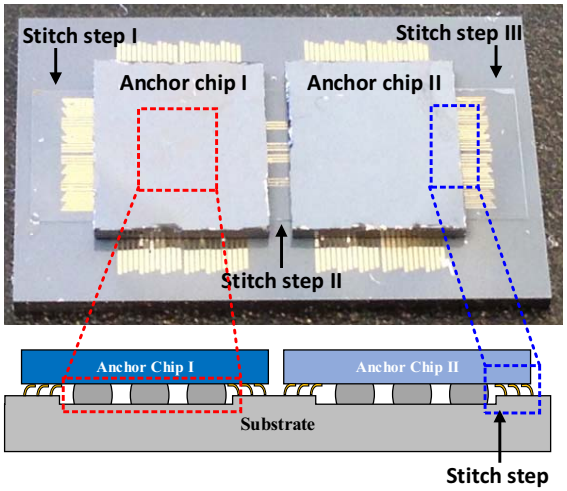


Fig. 4. Optical image and schematic of the assembled testbed

possible) and the fine-pitch CMIs are fabricated on the assembled dice. The fabricated solder bumps are 200 µm in pitch and approximately 50 µm in height while the fine-pitch CMIs are formed on a 20 µm in-line pitch and are approximately 40 µm in height. Fig. 3 shows the fabricated fine-pitch CMIs and solder bumps. The fine-pitch CMIs

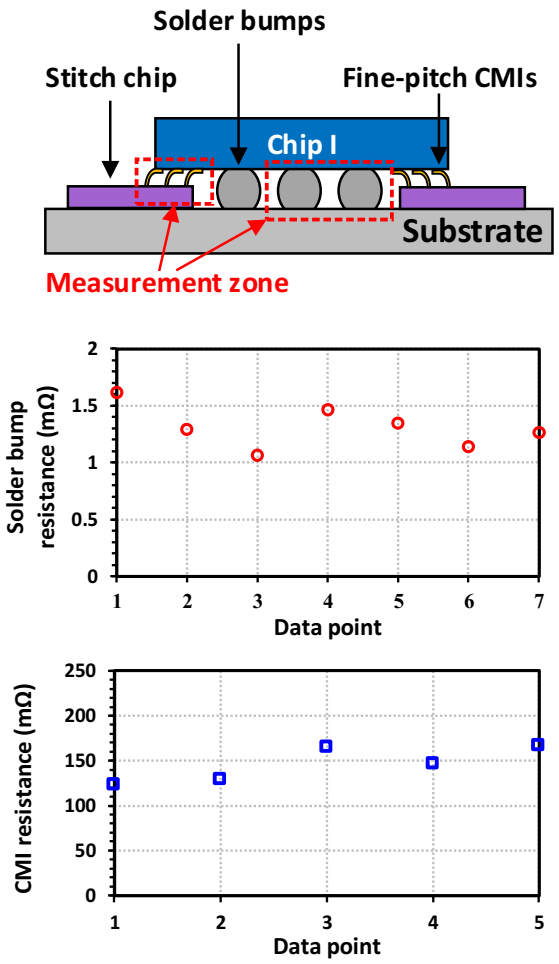


Fig. 5. Four-point resistance measurement results of the solder bumps and fine-pitch CMIs

provide high I/O density between the anchor chips concatenated through the stitch-chips. In order to uniformly distribute the stress along the CMI body during compression, an approximately tapered CMI body design is used; this can increase the vertical elastic range of motion. The upward-curved CMI geometry ensures that the tip of the CMI can maintain electrical and mechanical contact with the receiving pad during compression (i.e., assembly).

Optical image of the assembled testbed and schematic of the cross-sectional view are shown in Fig. 4. A Finetech Fine Placer Lambda flip-chip bonder is used to assemble the dice. In Fig. 4, the two anchor dice are placed side-by-side onto three stitch-chip regions on the substrate. Once the anchor dice are aligned to the substrate, the solder bumps are reflowed to provide both electrical and mechanical interconnection between the anchor dice and the substrate; the latter can provide enough contact force on the CMIs for reliable interconnection. As can be seen in Fig. 4, the center of the anchor die is bonded to the substrate using solder bumps, while two edges of the anchor die are suspended

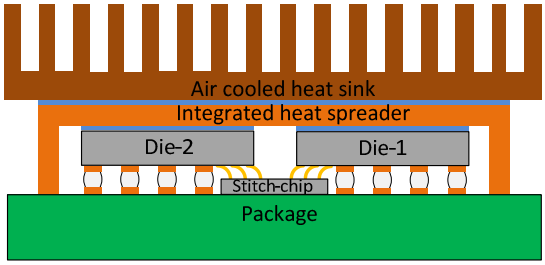


Fig. 6. Stitch-chip based simulation configuration

above the steps (i.e., the 'stitch-chips') and supported by the fine-pitch CMIs.

The four-point resistance values of the interconnections after assembly were measured using a Karl-Suss probe station. As shown in Fig. 5, the four-point resistance of each of the fine-pitch CMIs in contact with the gold pads on the stitch-chips was measured. The four-point resistance values of the solder bumps, which were reflowed during assembly, were measured as well. As shown in Fig. 5, the average resistance of the CMIs, including their contact resistance with the gold pads, is 146.31 mΩ, while the average resistance of the solder bumps is 1.31 mΩ. These four-point resistance measurement results confirm that the CMIs maintain reliable electrical connections between the anchor die and the stitch-chips after they are compressed downward and form a pressure-based contact. As noted earlier, owing to their mechanical flexibility, CMIs can compensate for any stitch-chip thickness variations or surface non-planarity of the substrate.

III. Thermal Evaluation of Stitch-Chip Based 2.5D Configurations

Fig. 6 shows stitch-chip based 2.5D integration with an integrated heat spreader and air cooled heat sink. In this section, we focus on a 2.5D integrated system of two anchor dice using the HIST platform.

A. Thermal Modeling Specifications

The thermal modeling framework used in this paper is reported in [16]. The model is based on the finite volume method and developed in MATLAB. The specifications used in the modeling of a HIST package containing two dice are shown in Table I. The specifications include the thickness and thermal conductivity of the different layers used in the HIST package. Moreover, the dice are assumed to be air-cooled. The boundary conditions used are similar to those in [16]. The power maps of the two emulated die (Die-1 and Die-2) are given in Fig. 7, which are based on Intel Core i7 processor and Altera Stratix FPGAs [16], respectively. The total power of Die-1 and Die-2 is 74.49W and 44.8W, respectively. The distance between the anchor dice is 0.5 mm. Recall that package-to-die interconnections are formed using bumps, while die-to-stitch-chip interconnects are formed using high-density CMIs.

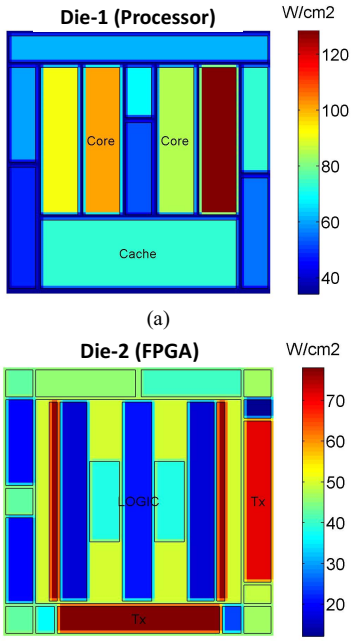


Fig. 7. Power density maps of each die. (a) Die-1, 74.49 W and (b) Die-2, 44.8 W

B. *Thermal Results*

Fig. 8 shows the thermal map of each die after thermal analysis. The dice have a maximum temperature of 102 °C and 89.5 °C, respectively. As evident from the figure, there is significant thermal coupling from the high-power die to the lower power die. There are two paths associated with the thermal coupling, with the primary coupling path being the atop heat spreader. For the 2.5D based integration technology under consideration, there is also a secondary thermal coupling path through the stitch-chip.

1) Thermal Coupling with Respect to Varying Power of Die-2

In this section, we sweep the power of Die-2 from 0 W to 74.5 W. Even though 0 W is unrealistic, we consider this case to emphasize the significance of thermal coupling between dice. For the 0 W Die-2 case, the temperature map in Die-2 is solely due to the thermal coupling through the heat spreader and the stitch-chip. Likewise, in the lower

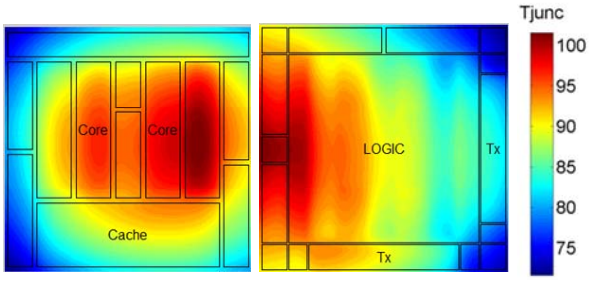


Fig. 8. Thermal profile of each die (a) Die-1 and (b) Die-2

Table I: Thermal Specifications

Layer	Conductivity (W/mK)		Thickness (μm)
	In-plane	Through-plane	
TIM	3		30
Heat spreader	400		1000
Chip-1 die	149		125
Chip-2 die	149		125
Stitch-chip	149		50
Underfill	3		N/A
ILD	61.17	1.62	5
Package	30.4	0.3	1000
Package-to-die bumps	60		70
Stitch-chip-to-die CMIs	60		20

power range, there is thermal coupling from Die-1 to Die-2. Fig. 10 reports the package thermal profile results for two different power levels. The bounding boxes define the boundary of each die. The stitch-chip is located between these two bounding boxes. We can see in the figure, depending on the power of Die-2, there is significant thermal coupling and heat spreading in the stitch-chip.

2) Die-thickness mismatch

Die thickness plays an important role in heat spreading. Increased die thickness reduces hotspot temperature. Typically, a heat spreader is attached on top of the chip using a thermal interface material (TIM). As such, in the configuration under consideration, we assume two TIM layers in the system. The first layer is between the heat sink and the heat spreader, and the second TIM layer is between the heat spreader and the top of the dice. In 2.5D heterogeneous integration, different chips can be fabricated by different vendors with different technologies. Moreover, state of the art memory chips in a 2.5D processor-memory

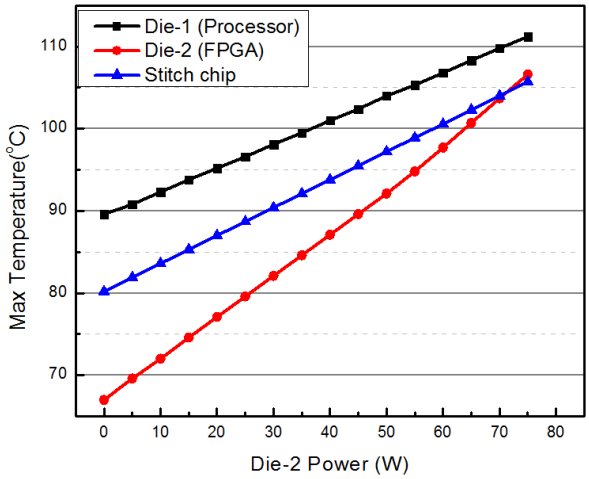
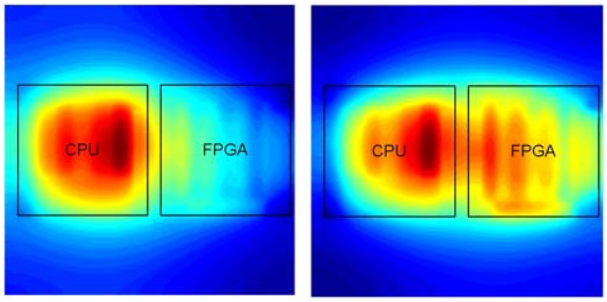


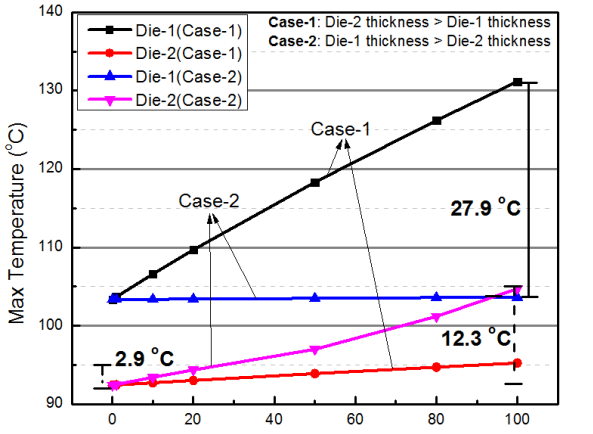
Fig. 9. Maximum temperature of different dice and the stitch-chip with respect to Die-2 power dissipation



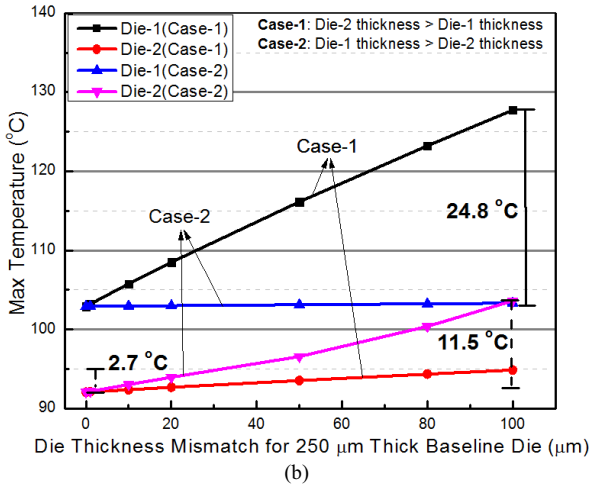
(a) (b)

Fig. 10. Thermal profile of (a) 74 W Die-1 and 44.8 W Die-2 HIST and (b) 74 W Die-1 and 74 W Die-2 HIST

integrated system typically contain multiple memory dice stacked together. Therefore, the aggregate thickness of the memory stack and the processor die may be different. Hence, it is necessary to fill the gap using TIM and/or copper (customized heat spreader [17]). To investigate the impact of die thickness mismatch, we make the following two assumptions. First, we assume that the only source of



(a)



(b)

Fig. 11. Impact of die-thickness mismatch for (a) 125 μm thick dice and (b) 250 μm thick dice.

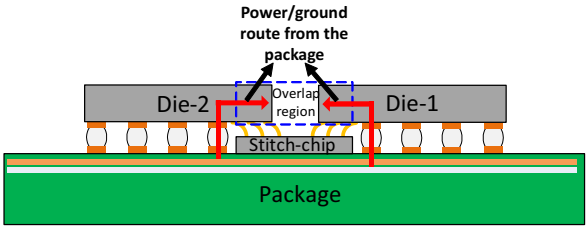


Fig. 12. Power delivery route from the package power/ground planes to the periphery of the dice

this mismatch is the absolute difference in the thicknesses of the dice. Second, except for the thicker die and unless otherwise specified, the rest of the dice in the system have default thickness values tabulated in the simulation parameters. We sweep the value of thickness mismatch from 0 μm to 100 μm. Moreover, we use two different baseline die thicknesses (125 μm and 250 μm) in the simulations. As evident from Fig. 11, if the high-power die is thinner than the low-power die, there can be as much as 28 °C increase in the maximum temperature. If the die thickness is doubled, the increase in maximum temperature reduces. However, the increase in temperature for thick dice can still be overwhelming.

IV. Power Delivery Network Analysis for Stitch-Chip Based 2.5D Integration

Stitch-chip is an enabling technology for high-density die-to-die interconnection. However, if no through stitch-chip vias are used, there may be no direct connection from the package power/ground planes to the active chips in the periphery. This may impact the power supply noise (PSN) in those regions [18]. Fig. 12 shows the power delivery route in the periphery of the anchor die owing to the overlap region with the stitch-chip.

A. DC IR-drop Simulation

For our power delivery network analysis, we use similar models and specifications as [18]. The stitch-chip is assumed to overlap with the active dice across an area of 0.5 mm × 6 mm in the periphery. Fig. 13 summarizes the IR-drop results for a simulation configuration specified in Fig. 12. Due to the absence of direct access from the package power/ground planes, Die-2 has higher PSN in the overlap region.

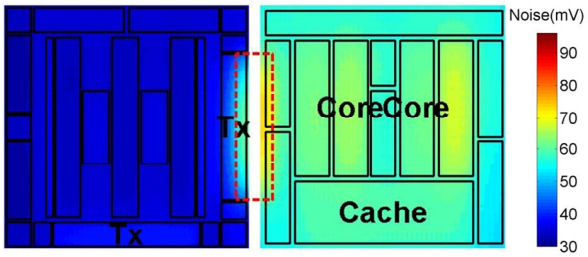


Fig. 13. The IR-drop profile of each die for a 0.5 mm × 6 mm overlap area with a stitch-chip

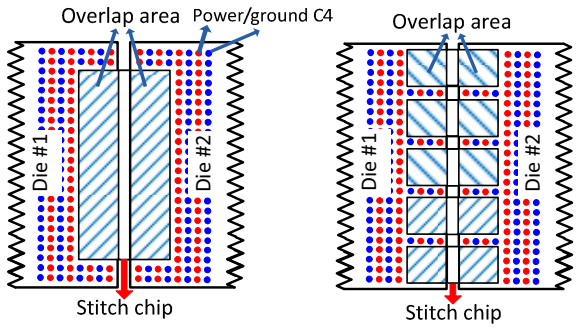


Fig. 14. (a) Single stitch-chip and (b) five stitch-chips for die-to-die interconnection

B. *Impact of Overlap Areas with Multiple Stitch-chips*

The PSN problem mentioned above is somewhat resolved by splitting the stitch-chip into multiple smaller stitch-chips [18]. The amount of overlap between the die and the stitch-chip negatively impacts the PSN. However, increasing this overlap will potentially increase the number of I/Os for die-to-die interconnection. To investigate the impact of I/O scaling, in this section, we vary the overlap area from baseline 0.5mm × 6 mm to 2.5 mm × 6 mm. An overlap area of 2.5 mm × 6 mm corresponds to a 5X increase in the number of I/Os for die-to-die interconnection compared to the baseline case (assuming I/O pitch is fixed). Moreover, we evaluate the benefits of multiple stitch-chips vs. a single large stitch-chip as well. Fig. 14 shows the overall configuration for this study. The figure shows the configuration with a stitch-chip overlap area of 0.5 mm × 6 mm. Fig. 14 (a) and (b) show the single stitch-chip and five stitch-chips cases, respectively. In both of the cases, the CMI pitch is assumed to be 40 µm. Fig. 15 presents the IR-drop analysis results for both of these configurations. To compare the results, we also included a 'Standalone' case

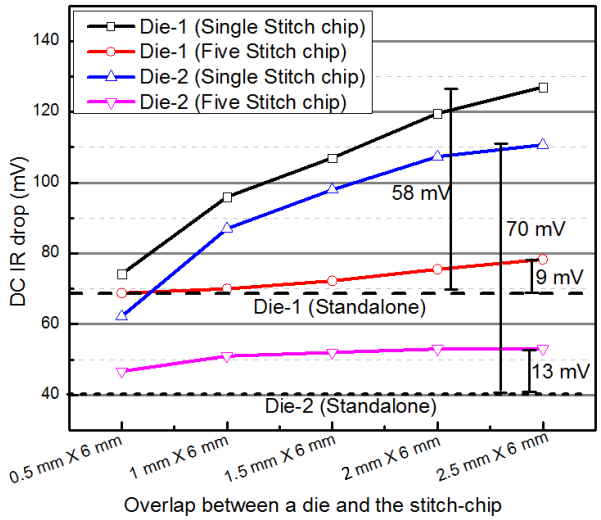


Fig. 15. Impact of the overlap area between a die and the stitch-chip on DC IR-drop of each die

where both dice are assembled on the package without any stitch-chips. We can see from the figure that the IR-drop results of the case using multiple stitch-chips is comparable to the standalone case. For both dice, the use of a single large stitch-chip yields the maximum IR-drop. This can be attributed to the larger effective distance from the power/ground interconnections to the periphery of the die. From the figure, for a 2.5 mm × 6 mm overlap area (5X die-to-die interconnections), there is a 58 mV and 70 mV increase in the IR-drops of Die-1 and the Die-2, respectively, compared to the standalone case. However, with stitch-chip splitting, both of the cases show comparable results to the standalone one.

V. Conclusion

This paper presents the fabrication and assembly process of a HIST integration concept using fine-pitch CMIs. Electrical characterization of the assembled testbed with the fine-pitch CMIs and solder bumps was performed, and measured results are presented to demonstrate early success. Four-point resistance measurement results of both solder bumps and fine-pitch CMIs show robust interconnection of two anchor chips through stitch-chips. HIST is proposed to achieve denser signaling between ICs in addition to providing a highly scalable and flexible 2.5D heterogeneous IC integration solution that extends beyond the reticle limits of traditional multi-die integration solutions. Thermal simulations of stitch-chip based configurations indicate that there is significant thermal coupling between dice. The results also indicate that the high-power die in a 2.5D package should be thicker, or equal to, the thickness of the low-power die. Power supply noise simulations show that the splitting of a large stitch-chip helps reduce the power supply noise of the chips by providing partial access to the package power/ground planes in the periphery of the chips.

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